STSM Report: Multi-Level Fault Simulator for Ionizing Effects

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COST Action: IC1204
STSM title: Multi-Level Fault Simulator for Ionizing Effects
Reference: ECOST-STSM-IC1204-150713-033450
STSM dates: from 15-07-2013 to 03-08-2013

Location: University of PASSAU, Passau, Germany
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I. BACKGROUND

Since the fault attack technique can be used to retrieve secrete information from secure circuit, fault simulation becomes a research "hot point" for secure design. In this STSM project, the visitor, LU Feng, is doing this visiting research as part of his PhD studies on a project for Multi-Level Fault Simulator for Ionizing Effects. As a multi-level simulator, it has two delay calculation methods for logic-level simulation and electrical-level simulation. Decreased error between two delay calculation methods can improve the simulation precision. The host group has a research direction for delay fault simulation, which concentrate on delay calculation for logic-level simulation. The goal of this visit is to try to improve our simulator by using other delay calculation method.

1. tLIFTING: Multi-level fault simulator

Our simulator tLIFTING is based on a combination of electrical-level simulations (HSPICE) for the sub-circuit affected by the fault and the propagation paths, and logic-level simulation for the rest of the circuit. This multi-level simulation can be turned for saving computational time or for improving the measurement accuracy. However, due to different delay of logic-level simulation and electrical-level simulation, tLIFTING simulation results do not exactly match in time and duration the one generated by pure HSPICE simulation. For sequential logic block, this propagation delay difference may cause the different latched value at flip-flops and the simulation error (Fig. 1).

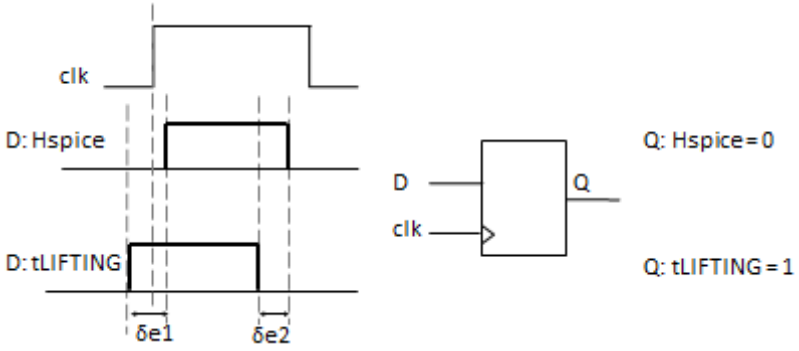

Figure 1: Propagation delay difference caused simulation error for sequential logic

2. Delay fault simulator

JIANG Jie, Ph.D. candidate of Prof. Ilia Polian, developed a simulator for IR-Drop Induced Delays simulation. The current draw and delay of a switching gate depend on the power supply levels, which are likely to be affected by IR-drop induced by neighboring gates, and on the load capacitance of the gate. So, its delay model depends on three parameters: load capacitance, supply and input swings. Fig. 2 shows the definition of these three parameters.

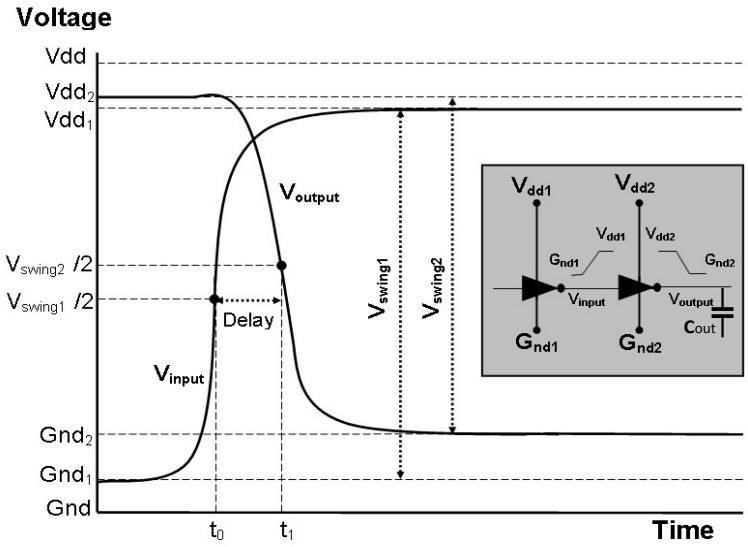

Figure 2: The parameters definition of delay model

Here the input swing and supply swing (Vswing1 and Vswing2) are defined as follow:

$$Vswing1 = Vdd1 - Gnd1 \quad (1)$$

$$Vswing2 = Vdd2 - Gnd2 \quad (2)$$

For its delay model, the considered gate can be affected by a voltage drop on the power and/or the ground supplies, which impacts the current draw and delay. It must be considered that the upstream gate may also be affected by a voltage drop, which also impacts the behavior of the considered gate. The voltage swings of the upstream gate (input swing) and the considered gate (supply swing). The input capacitances of the downstream gates, which are connected to the considered gate, are abstraced and accumulated as the load capacitance Cout of the considered gate.

II. DETAILED WORK DONE DURING THE VISIT

Comparison of the different delay calculation results

The IR-Drop induced delays model depends on input and supply swings, but, if we fix the Vdd and Gnd of all the gates, the calculated delays will represent the normal situations. At the first step of this visit, we calculated the gate delays for a test circuit (c17 with 45nm technique) with the fixed supply voltage (Vdd = 1v and Gnd = 0v) and compared these delays with the HSPICE simulation result and the standard delay format (SDF) file. Table 1 shows all the gate delays calculated by different methods for test circuit c17.

Table 1. Comparison of the different delay calculation results for tech. 45nm

Gate	out_capa (ff)			SDF (ps)	HSPICE (ps)	IR_Drop (ps)
NAND2_X1 U5	NON	A1 to ZN	0 to 1	10	9.2	5.57576704
			1 to 0	9	9.09	3.08273101
		A2 to ZN	0 to 1	12	11.2	5.72510624
			1 to 0	11	10.7	4.89805222
NAND2_X1	1.664199	A1 to ZN	0 to 1	12	11.6	8.04600811
			1 to 0	11	10.2	4.37284327

U6		A2 to ZN	0 to 1	14	14.2	6.93516779
			1 to 0	12	11.7	6.21643543
NAND2_X1 U7	1.599032	A1 to ZN	0 to 1	15	13.5	8.04600811
			1 to 0	13	13	4.37284327
		A2 to ZN	0 to 1	14	13.9	6.93516779
			1 to 0	12	11.6	6.21643543
NAND2_X1 U8	1.599032	A1 to ZN	0 to 1	12	11.5	8.04600811
			1 to 0	11	10	4.37284327
		A2 to ZN	0 to 1	14	13.9	6.93516779
			1 to 0	12	11.6	6.21643543
NOR2_X1 U2	1.714471	A1 to ZN	0 to 1	24	22.7	8.08959103
			1 to 0	9	8.26	8.39511967
		A2 to ZN	0 to 1	29	27.2	5.31801176
			1 to 0	10	9.07	5.28930378
NOR2_X1 U4	NON	A1 to ZN	0 to 1	14	12.7	6.47901535
			1 to 0	7	5.84	6.6410594
		A2 to ZN	0 to 1	19	17.2	3.7360878
			1 to 0	9	8.39	3.60513449
NOR2_X1 U9	1.651345	A1 to ZN	0 to 1	24	22.3	8.08959103
			1 to 0	6	6	8.39511967
		A2 to ZN	0 to 1	27	26.4	5.31801176
			1 to 0	7	6.93	5.28930378
INV_X1 U1	1.651345	A to ZN	0 to 1	10	9.7	3.99733448
			1 to 0	5	5.38	4.91144991
INV_X1 U3	1.714471	A to ZN	0 to 1	10	9.86	3.99733448
			1 to 0	5	5.47	4.91144991

Unfortunately, the calculated delays by IR_Drop delay model are less accurate than the SDF data. There are two principal reasons for of this error,

1. The IR_Drop delay model is considered the voltage drop affects of the upstream gate, but it is difficult to summarize the upstream gate effects for all types of standard gates. The model is studied and deduced with a inverter as the upstream gate.
2. Since the variation of the delay is also in function of the load capacitance, the load capacitance values is assumed from one to five times the elementary equivalent capacitance of an inverter, for positive and negative transition edges and for all standard gates. This assumption is just a compromise between the complexity of the algorithm and the accuracy.

These two compromises cause the precision losing of the IR_Drop delay model. No the other hand, the SDF date are calculated with the input slope which corresponds to upstream gate and with the more accurate load capacitance for downstream gates. So, for the second work step, I studied the algorithm for standard delay format.

Nonlinear delay model

Standard Delay Format (SDF) is an IEEE standard for the representation and interpretation of timing data for use at any stage of an electronic design process. SDF delay data will vary according to the algorithm. For us, our SDF files are generated by “Synopsys Design Compiler” (Version "E-2010.12-SP5") with the nonlinear delay model (NLDM) algorithm. The nonlinear delay model looks up the delay from a table based on the load capacitance and the input slope. Separate tables are used to lookup rising and falling delay and output slope for downstream gate(s). And all the tables for each gate in a standard cell library are stored in a .lib file. Table 2 shows an example of nonlinear delay model for falling delay of an inverter (INV_X1) of 45nm technique library.

Table 2. Falling Nonlinear Delay Model for Inverter INV_X1

INV_X1 cell_fall [ns]		Input Net Transition [ns]						
		0.00117378	0.00472397	0.0171859	0.0409838	0.0780596	0.130081	0.198535
Total Output Net Capacitance [ff]	0.365616	0.00334769	0.00529785	0.00763425	0.0122592	0.0214710	0.0398747	0.0766650
	1.897810	0.00461096	0.00678237	0.00912396	0.0137631	0.0229885	0.0413991	0.0781923
	3.795620	0.00565781	0.00963029	0.0133910	0.0192072	0.0284937	0.0468495	0.0836153
	7.591250	0.00501217	0.0107451	0.0162361	0.0248924	0.0380191	0.0575991	0.0941587
	15.182500	0.00228759	0.00977055	0.0169885	0.0284204	0.0459573	0.0721436	0.111006
	30.365000	-0.00275926	0.00641510	0.0153503	0.0295626	0.0514378	0.0844139	0.133051
	60.730000	-0.0102639	0.000468768	0.0110680	0.0280603	0.0542902	0.0939467	0.152970

The SDF generator uses interpolation when a specific load capacitance and/or slope are not in the table. Lookup tables of the same type are stored in library for output transitions, and these output transitions will be transmitted to their fan-out gate(s) as the input transition parameter.

I measured the errors between NLDM results and the golden results from HSPICE simulation. And for correlating the errors with the technique dimension, the test circuit is simulated by HSPICE with two technique libraries (45nm and AMS c35). Table 3 shows the delays for same test circuit c17 with the technique of 135nm.

Table 3. Comparison of the NLDM delay and HSPICE calculation results for tech. c35

	out_capa (ff)			SDF (ps)	HSPICE (ps)
NAND20 U5	NON	A1 to ZN	0 to 1	214	109
			1 to 0	106	41.5
		A2 to ZN	0 to 1	227	163
			1 to 0	87	46.3
NAND20 U6	5.672	A1 to ZN	0 to 1	204	201
			1 to 0	96	92.8
		A2 to ZN	0 to 1	233	240
			1 to 0	106	88.7
NAND20 U7	4.063	A1 to ZN	0 to 1	233	170
			1 to 0	131	78.4
		A2 to ZN	0 to 1	221	223
			1 to 0	101	77.1
NAND20 U8	4.063	A1 to ZN	0 to 1	192	183
			1 to 0	91	79.2
		A2 to ZN	0 to 1	221	223
			1 to 0	101	77.1
NOR20 U2	5.453	A1 to ZN	0 to 1	239	106
			1 to 0	230	113
		A2 to ZN	0 to 1	227	88.7
			1 to 0	200	65.3
NOR20 U4	NON	A1 to ZN	0 to 1	208	91.1
			1 to 0	202	90.6
		A2 to ZN	0 to 1	195	65
			1 to 0	167	57.6
NOR20 U9	5.801	A1 to ZN	0 to 1	212	95.4
			1 to 0	163	98.5
		A2 to ZN	0 to 1	184	72.5
			1 to 0	136	60.7
INV0 U1	5.801	A to ZN	0 to 1	192	175
			1 to 0	120	98.7
INV0 U3	5.453	A to ZN	0 to 1	192	172
			1 to 0	120	95.4

By comparing the two tables (Table 1 and Table 3), it can be concluded that NLDM is more accurate for the new technique of which the standard cells are downsized in area.

NLDM limitation for the different input slope of injected fault pulse

As the SDF file is fixed for a given circuit, and the delays of each gate are calculated with the upstream gate output slope. But when a fault pulse is injected into test circuit, if the rising and/or falling slopes are more different from their upstream gate's output slope, the propagation delay of this fault pulse would no longer comply with the SDF values, and this difference may be accumulated by downstream gates with the changed output transition (Figure 3).

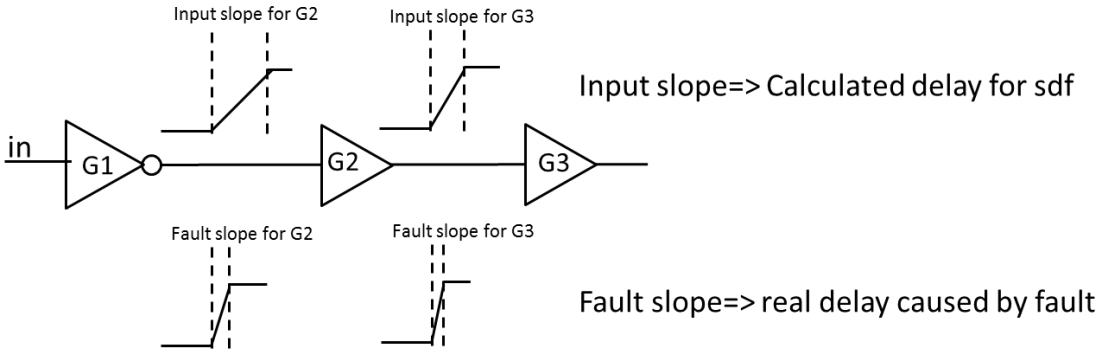

Figure 3: Injected fault pulse induced delay error

III. FUTURE WORKS

During this visit, we compared the different delay calculation methods and studied the NLDM. For the future works, there are two points for improving our multi-level fault simulator and one proposal for the IR-Drop induced delays model:

1. Since there are errors between NLDM lookup table and HSPICE calculation, whether we can improve the SDF file accuracy by recalculating the lookup table data with HSPICE.
2. In our multi-level simulator, the faulty sub-circuit is simulated at electrical-level, but the stimuli are calculated from the logic-level simulation without slope information. So, the accuracy of multi-level simulation can be increased by adding the input slope into the sub-circuit stimuli.
3. From the Table 1, we can find that the calculated result by the IR-Drop induced delays model is a little different from the HSPICE result, when there is not any power perturbation. This is because that, in this model, the upstream gate type is not considered and that the load capacitances are not very accurate. But according to the original IR-Drop induced delays model [1], the delay increases linearly when the supply swing or input swing of the gate decreases (the other variable parameters being constant at nominal value)(Fig.4).

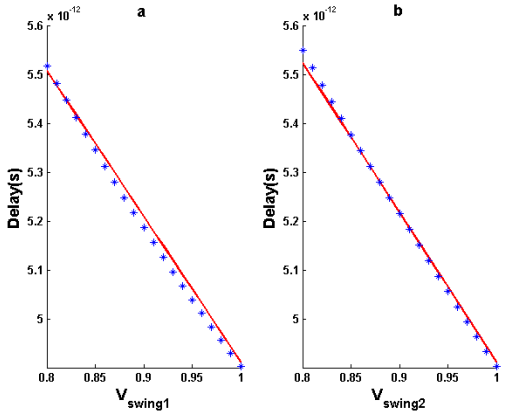

Figure 4: Variation of the inverter delay as a function of the: a) input swing; b) power swing.

So I propose there to re-verify whether the relationship between the delay and the supply/input swing is linear for all the standard cells. If so, a new polynomial delay model which is based on NLDM may improve the accuracy for IR-Drop induced delays fault simulation.

Reference

[1] M. Aparicio, Mariane Comte, Florence Azaïs, Michel Renovell, J. Jiang, Ilia Polian, Bernd Becker: Pre-characterization procedure for a mixed mode simulation of IR-drop induced delays. LATW 2013: 1-6